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P.001

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FEB 20 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Musahiro Ishida, et al.  
Serial No.: 09/699,077  
Filing Date: October 27, 2000  
Title: Method and Apparatus for  
Fault Simulation of  
Semiconductor Integrated  
Circuit

Examiner: Ayal Sharon

Art Unit: 2123

OFFICIAL

*Handwritten signature and date: 2-26-04*

February 19, 2004  
San Francisco, California

Mail Stop Non-Fee Amendment  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

This communication is submitted in response to the office action mailed November 20, 2003  
(referred to herein as "Office Action").